REMARKS

Claims 1-24 are pending. The examiner has acknowledged that claims 3, 8-10 and 14 are directed to allowable subject matter. Accordingly, claims 3, 8, and 14 have been rewritten as independent claims and are deemed allowable. Claims 9 and 10 depend from claim 8 and are also deemed allowable. New claims 23 and 24 have been added. Reconsideration of this application in light of the above amendments and the following remarks is requested.

Objections to Drawings under 37 CFR 1.83(a)

Claim 1 has been amended to recite "an ultra thin oxide material," rather than a "dielectric material." Accordingly, Applicant requests that the rejection of claim 1 under 37 CFR 1.83(a) be withdrawn.

With respect to the rejection of claim 12 under 37 CFR 1.83(a), Applicant submits that Figs. 5 and 6 clearly present multiple fingers and that, in conjunction with the structures illustrated in Figs. 1 and 2, the subject matter of claim 12 is shown in the claims. Accordingly, Application requests that the rejection of claim 12 be withdrawn.

Rejections under 35 U.S.C. § 102

As the PTO provides in MPEP § 2131, "[t]o anticipate a claim, the reference must teach every element of the claim...." (emphasis added). Therefore, each reference applied under 35 U.S.C. § 102 must disclose all of the elements of the claims to sustain the rejection. Accordingly, Applicant respectfully traverses this rejection on the following grounds.

Claims 1, 2, 4-7, and 11

Claim 1 stands rejected under 35 U.S.C. § 102 in light of U.S. Patent No. 6,373,109 to Ahn ("Ahn"), U.S. Patent No. 6,329,287 to Gadepally ("Gadepally"), and U.S. Patent Publication No. 2002/0053704 to Avery et al. ("Avery").

Claim 1, as amended, recites a deep submicron electrostatic discharge (ESD) protection structure comprising first and second electrodes separated by an ultra thin oxide material; a silicide covered, grounded gate positioned above the ultra thin oxide material; a source positioned proximate to the first electrode; and a drain positioned proximate to the second electrode and covered by a silicide layer, wherein the silicide layer enhances ESD protection provided by the structure.

Applicant can find no teaching or suggestion of each element in Ahn, Gadepally, or Avery as required by MPEP § 2131. More specifically, Ahn teaches that "it is noted that the dummy gate electrode 124c is an electrode which does not receive a voltage when operating the semiconductor device and simply formed to prevent a silicide layer from being formed on impurity layers 126, that is drains of the ESD protecting device." (col. 3, lines 58-62) (emphasis added). Accordingly, Ahn fails to teach or suggest Applicant's claimed invention as recited in claim 1, and claim 1 is allowable over the cited reference for at least this reason.

Contrary to the Examiner's statement that Gadepally "discloses a deep submicron electrostatic discharge (ESD) protection structure," Gadepally simply states that "[i]t can be desirable to form integrated circuits that include both MOS transistors structures with metal salicide layers (i.e., metal salicide regions) and MOS transistor structures without metal salicide layers (i.e., metal salicide exclusion regions). For example, it is often beneficial to form input/output (I/O) MOS transistor structures without metal salicide layers in order to provide a relatively high resistance I/O path for electrostatic discharge (ESD) protection." (col. 1, line 66 – col. 2, line 6). Furthermore, Gadepally fails to teach or suggest, among other elements, a silicide covered, grounded gate positioned above the ultra thin oxide material as recited in claim 1, and claim 1 is allowable over the cited reference for at least this reason.

With respect to Avery, Applicant cannot find any teaching or suggestion as to a silicide covered, grounded gate positioned above the ultra thin oxide material as recited in claim 1. Accordingly, Avery fails to teach or suggest every element of claim 1 as required by MPEP § 2131, and claim 1 is allowable over the cited reference.

Claims 2, 4-7, and 11 depend from and further limit claim 1 and are allowable for at least the same reasons as claim 1.

Claims 12 , 13, and 15-17

Claim 12 stands rejected under 35 U.S.C. § 102 in light of Avery. Claim 12, as amended, recites in part first and second silicide covered, grounded gates positioned above a thin oxide material. As described above, Applicant can find no teaching or suggestion of this element in Avery as required by MPEP § 2131, and claim 12 is allowable over the cited reference for at least this reason. Claims 13 and 15-17 depend from and further limit claim 12 and are allowable for at least the same reason as claim 12.

Claims 18-22

Claim 18 stands rejected under 35 U.S.C. § 102 in light of Avery. Claim 18, as amended, recites in part "forming a silicide covered, grounded polysilicon gate structure above the gate oxide layer." Applicant can find no teaching or suggestion of this element in Avery as required by MPEP § 2131, and claim 18 is allowable over the cited reference for at least this reason. Claims 19-22 depend from and further limit claim 18 and are allowable for at least the same reason as claim 18.

New claims 23 and 24

New claim 23 recites a deep submicron electrostatic discharge (ESD) protection structure comprising: a thin oxide layer formed on a substrate; a silicide covered, grounded gate positioned on the thin oxide layer; a silicide covered source positioned proximate to the thin oxide layer on one side of the grounded gate; and a silicide covered drain positioned proximate to the thin oxide layer on the side of the grounded gate opposite the source.

Applicant submits that the cited references fail to teach or suggest each element of claim 23 as required by MPEP § 2131, and claim 23 is allowable over the cited references. New claim 24 depends from and further limits claim 23 and is allowable for at least the same reason as claim 23.

CONCLUSION

It is respectfully submitted that all the claims in the application are in condition for allowance. Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the below listed telephone number.

Respectfully submitted,

T. F. Bliss

Timothy F. Bliss
Registration No. 50,925

Dated: October 25, 2004
HAYNES AND BOONE, LLP
901 Main Street, Suite 3100
Dallas, Texas 75202-3789
Telephone: 972/739-8638
Facsimile: 214/651-5940
Client Matter No.: 24061.27
R80308

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 25, 2004.

Gayle Conner

Gayle Conner